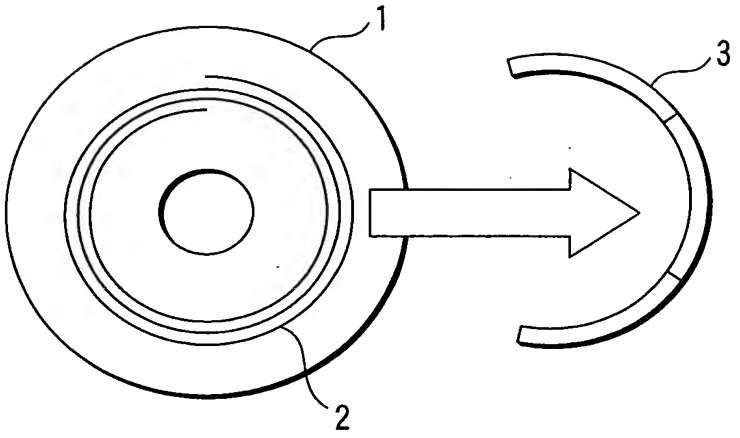


FIG. 1

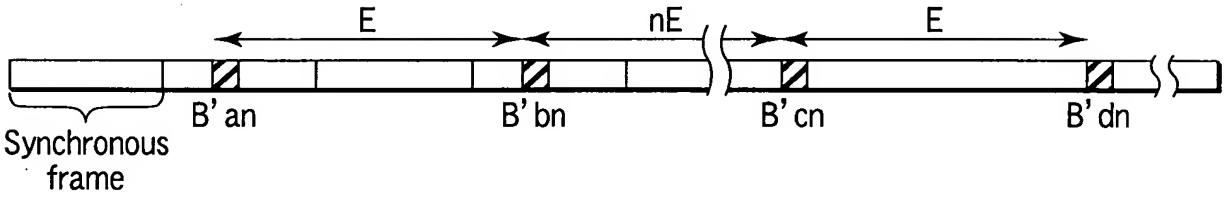


FIG. 3

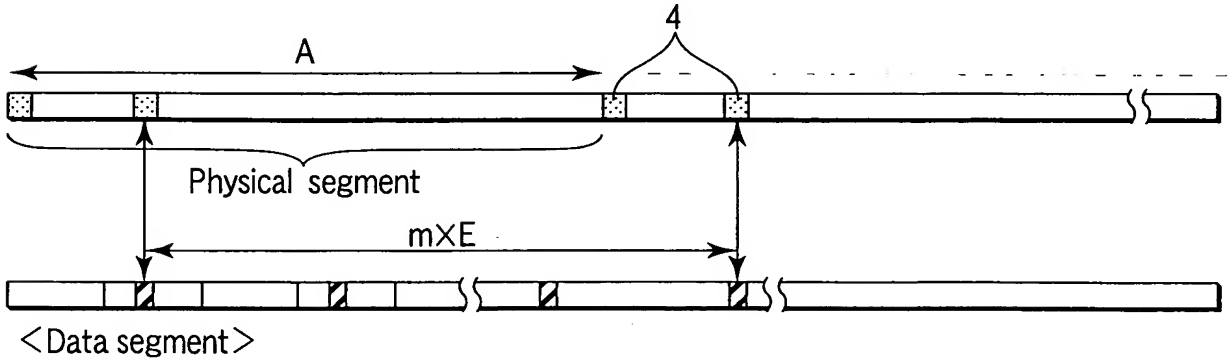


FIG. 4

FIG. 2A

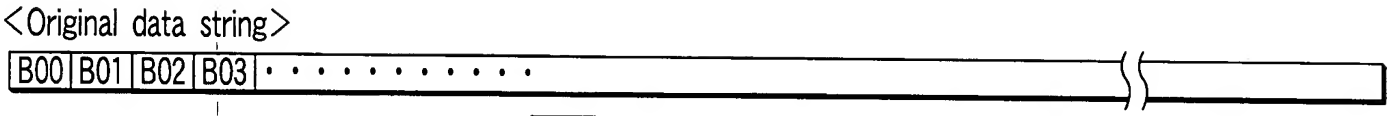


FIG. 2B

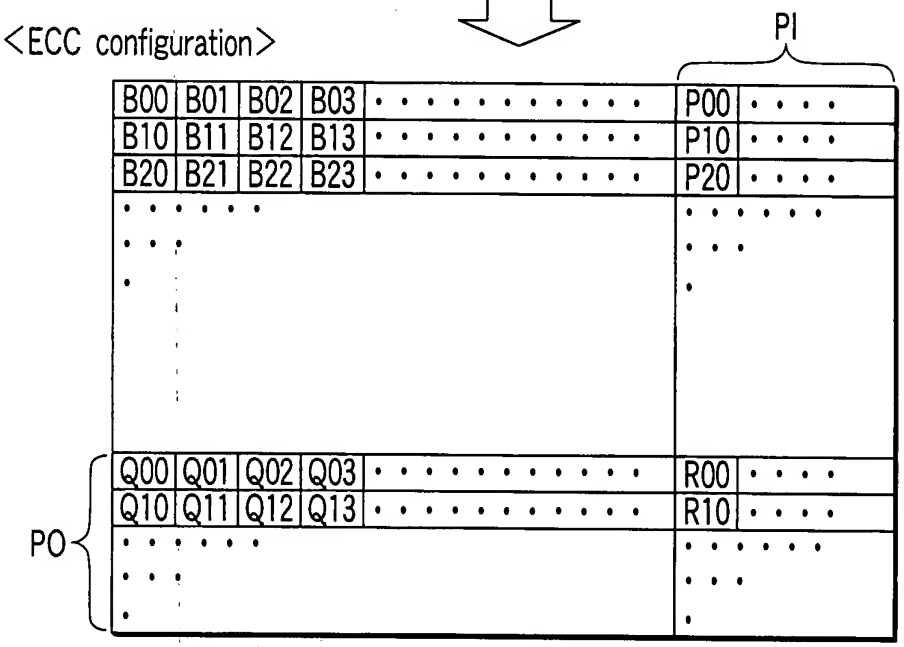


FIG. 2C

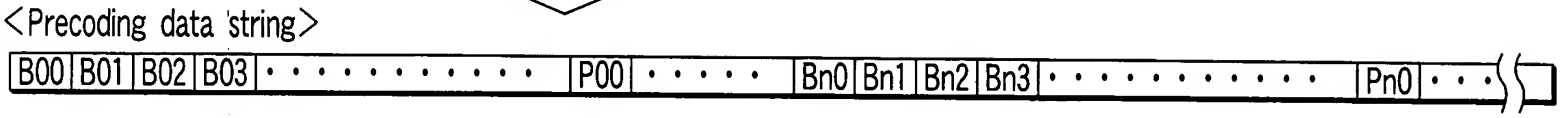
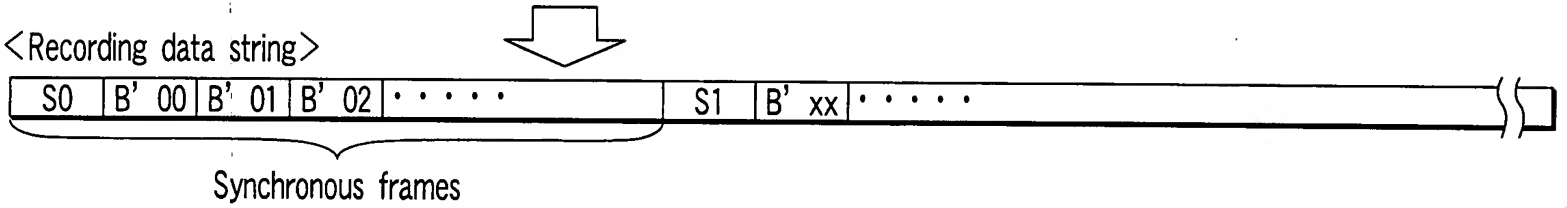


FIG. 2D



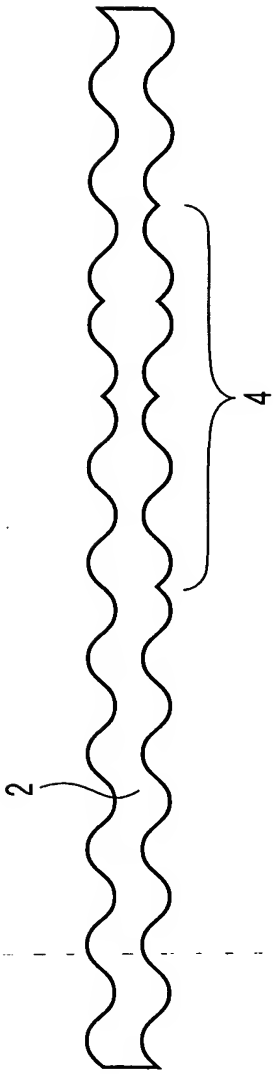


FIG. 5

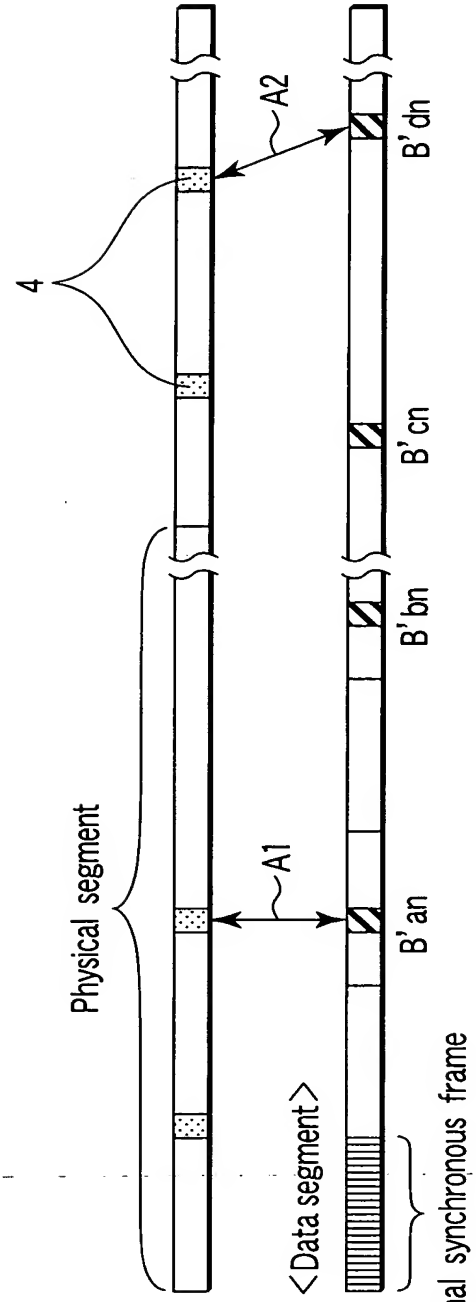


FIG. 6

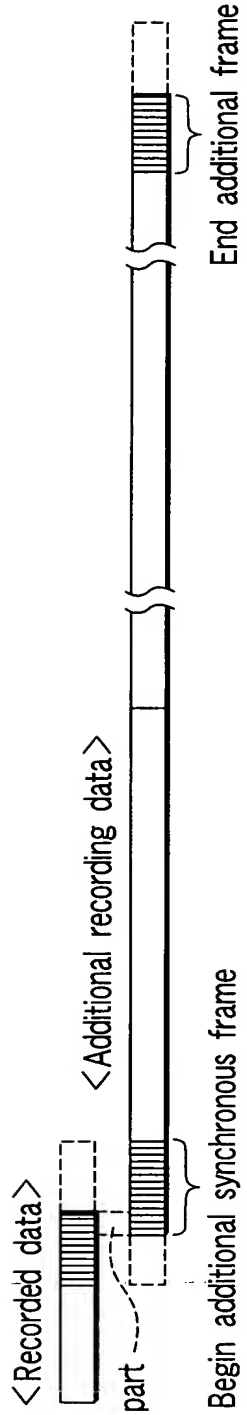


FIG. 7

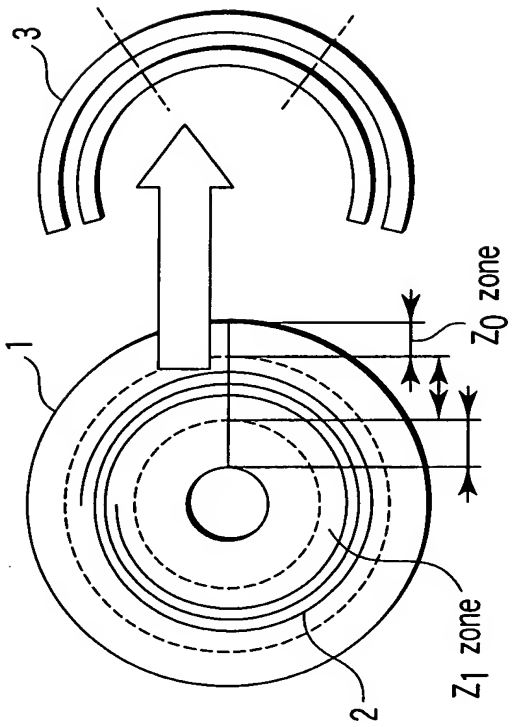

3
1
Z_0 zone
Z_1 zone
2

FIG. 8

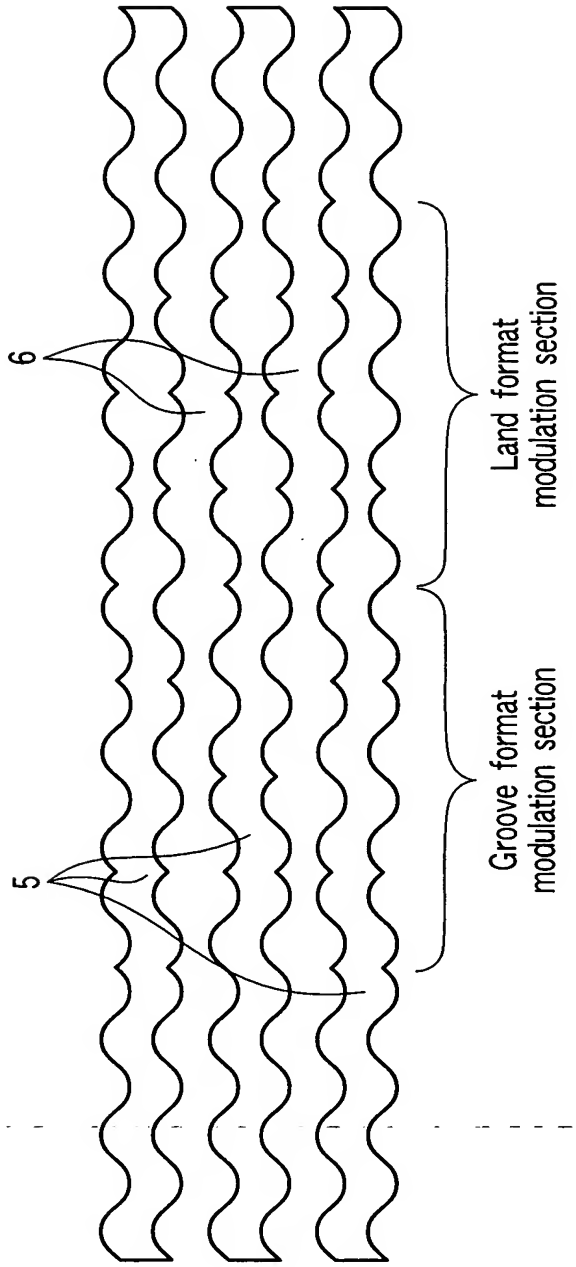

6
5
Land format modulation section
Groove format modulation section

FIG. 9

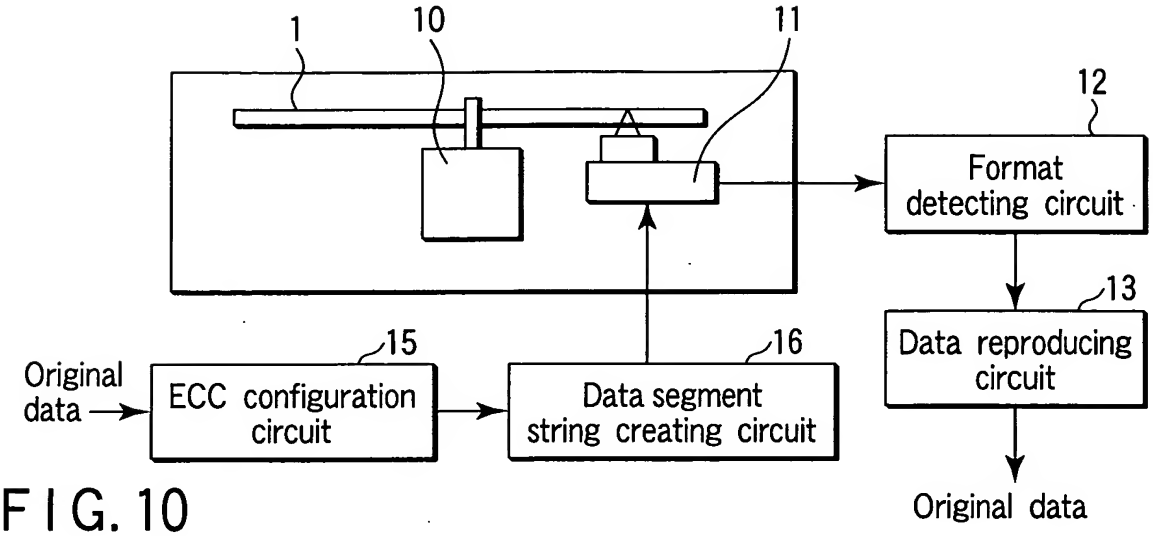


FIG. 10

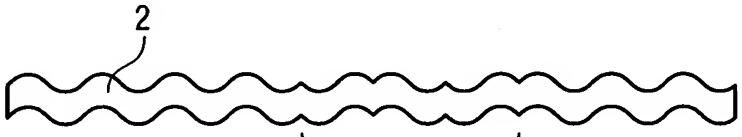


FIG. 11A

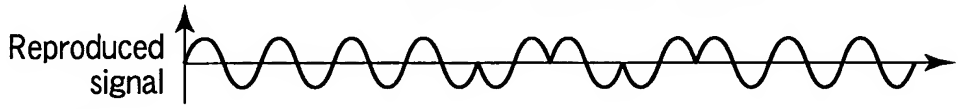


FIG. 11B

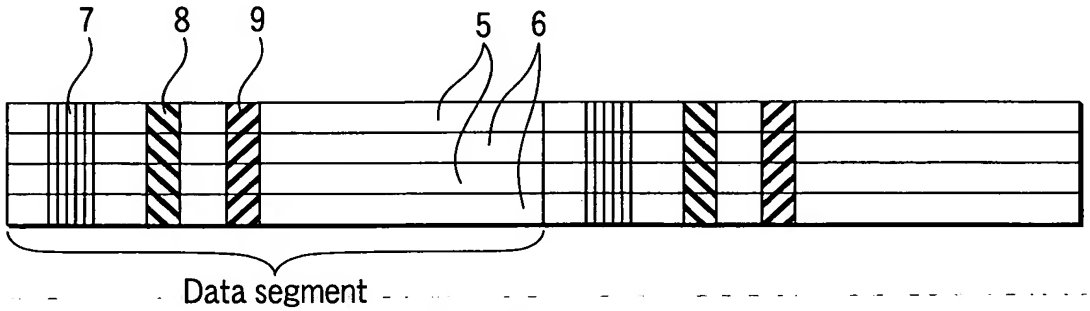


FIG. 12

FIG. 13

Binary code	Gray code
000000	000000
000001	000001
000010	000011
000011	000010
000100	000110
000101	000111
000110	001111

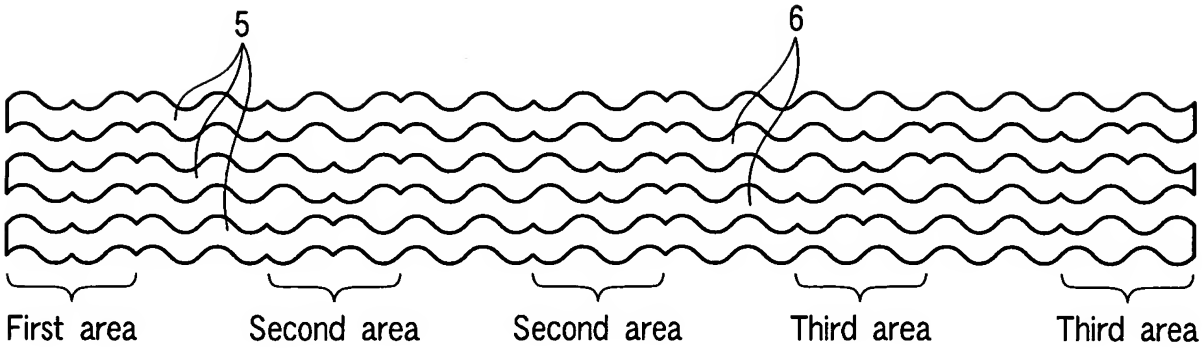


FIG. 14

FIG. 15A

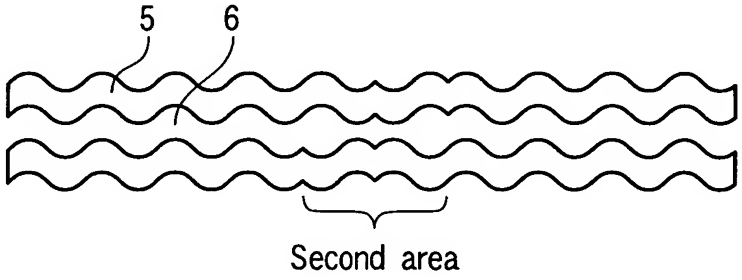


FIG. 15B

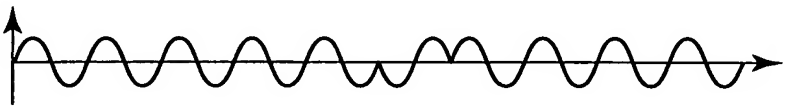


FIG. 15C

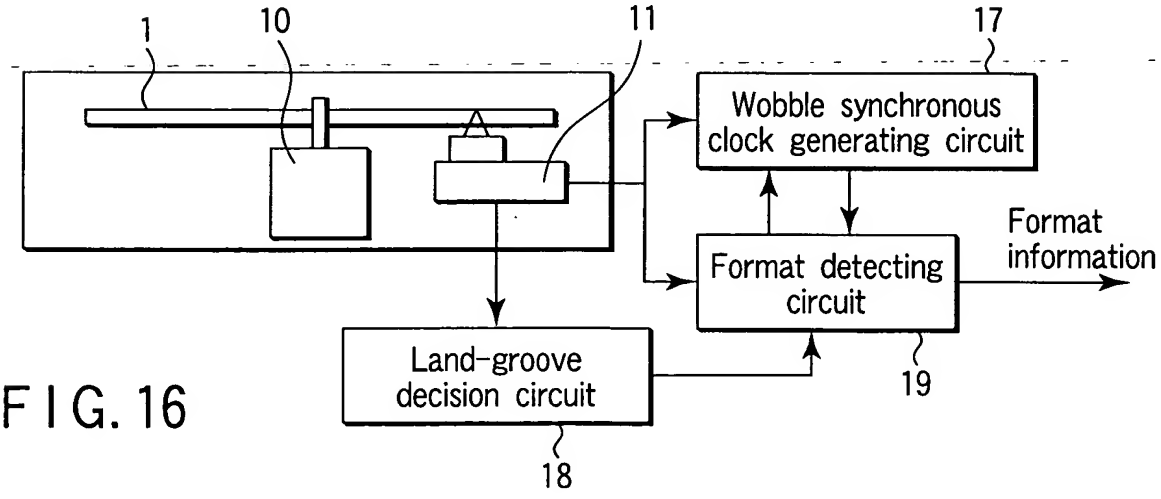


FIG. 16

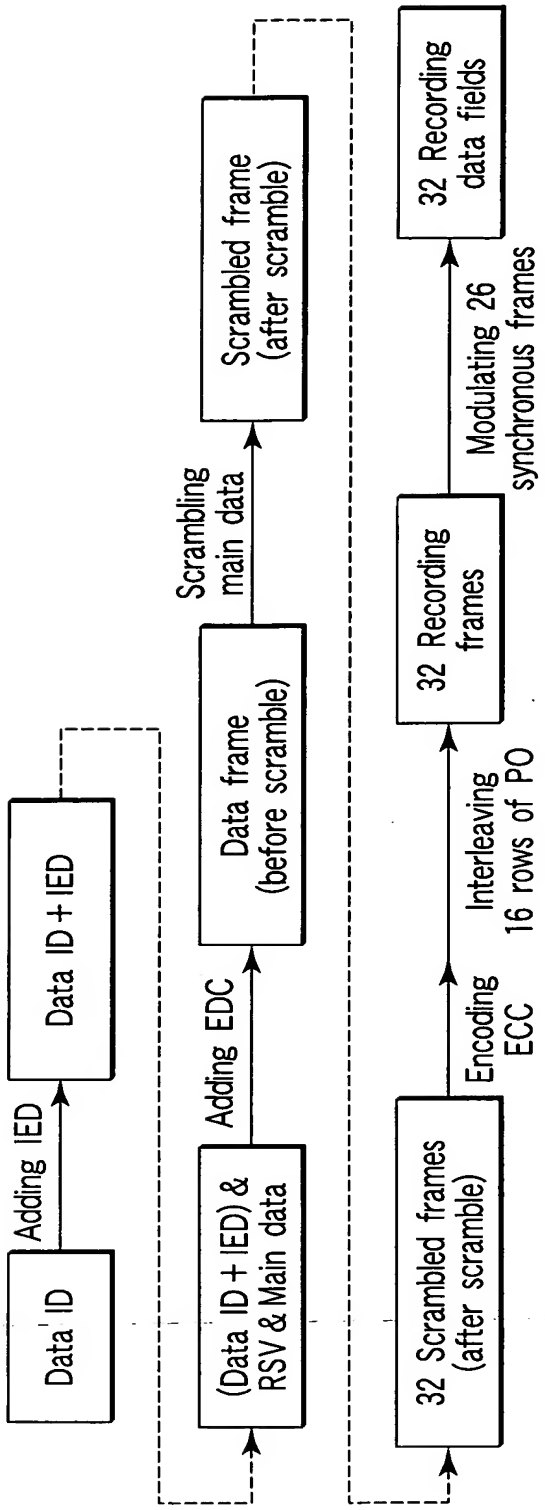

Data ID
Adding IED
Data ID + IED
(Data ID + IED) & RSV & Main data
Adding EDC
Data frame (before scramble)
Scrambling main data
Scrambled frame (after scramble)
32 Scrambled frames (after scramble)
Encoding ECC
Interleaving 16 rows of PO
32 Recording frames
Modulating 26 synchronous frames
32 Recording data fields

FIG. 17

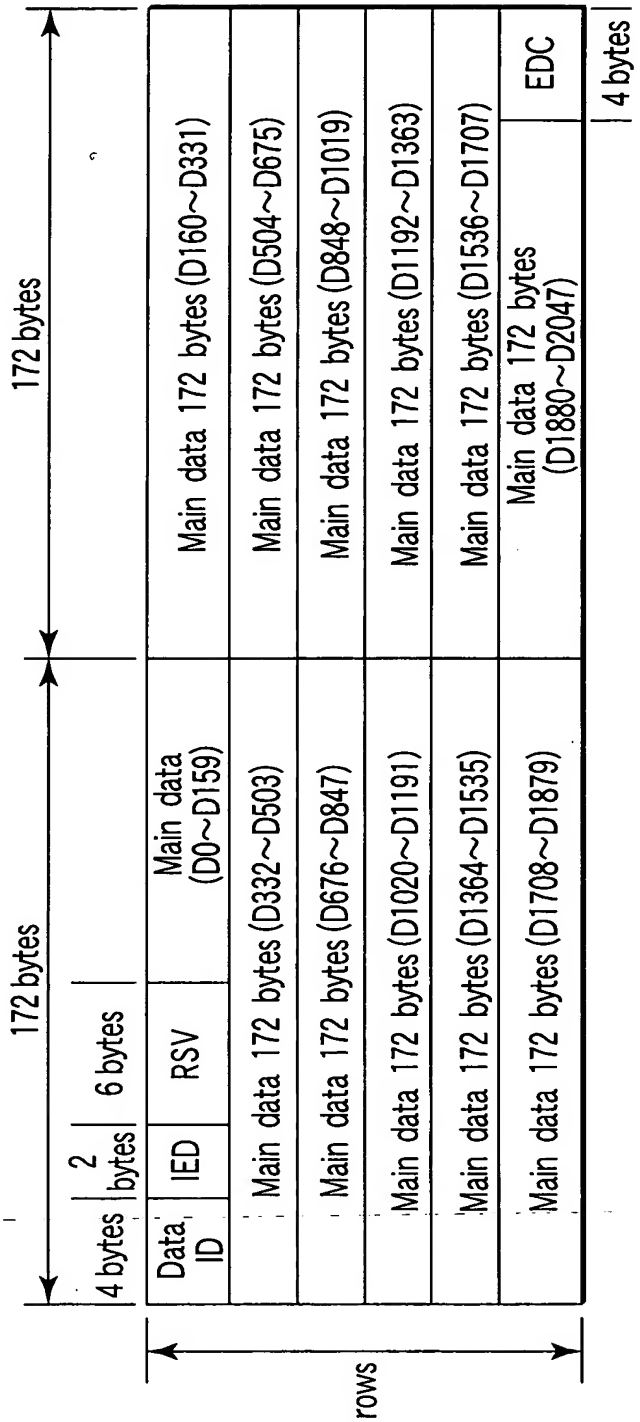

172 bytes
172 bytes
4 bytes
Data ID
2 bytes
IED
6 bytes
RSV
Main data (D0~D159)
Main data 172 bytes (D160~D331)
Main data 172 bytes (D332~D503)
Main data 172 bytes (D504~D675)
Main data 172 bytes (D676~D847)
Main data 172 bytes (D848~D1019)
Main data 172 bytes (D1020~D1191)
Main data 172 bytes (D1192~D1363)
Main data 172 bytes (D1364~D1535)
Main data 172 bytes (D1536~D1707)
Main data 172 bytes (D1708~D1879)
Main data 172 bytes (D1880~D2047)
EDC
4 bytes
6 rows

FIG. 18

FIG. 19

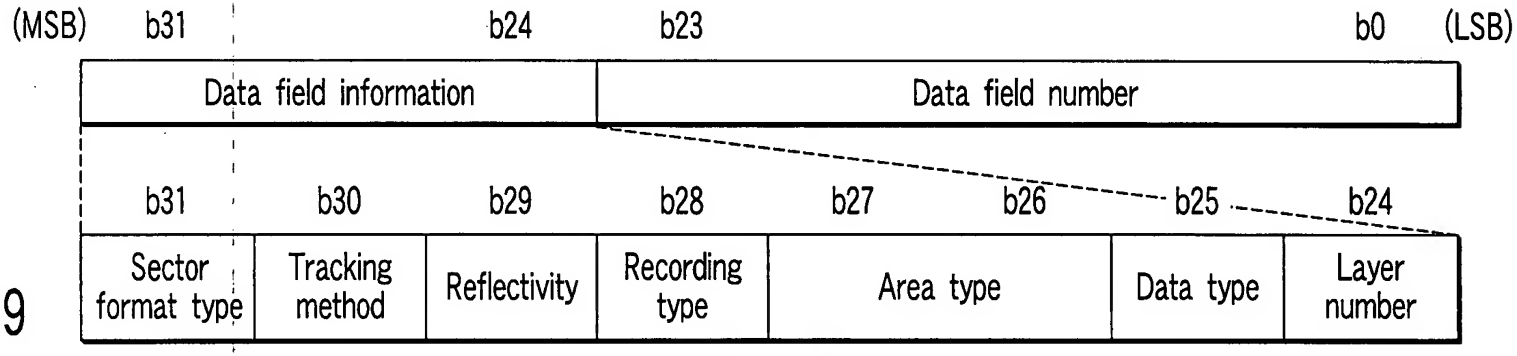
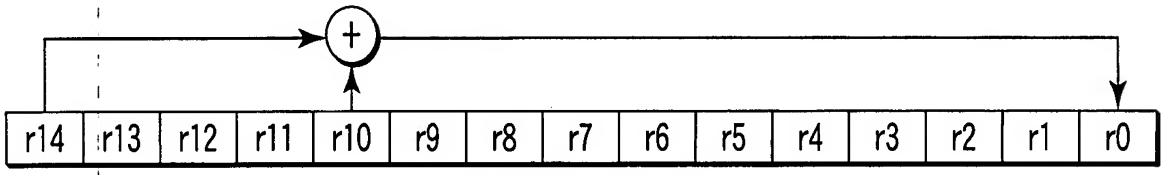


FIG. 20A

Initial preset number	Initial preset value	Initial preset number	Initial preset value
0h	0001h	8h	0010h
1h	5500h	9h	5000h
2h	0002h	0Ah	0020h
3h	2A00h	0Bh	2001h
4h	0004h	0Ch	0040h
5h	5400h	0Dh	4002h
6h	0008h	0Eh	0080h
7h	2800h	0Fh	0005h

Initial value of shift register

FIG. 20B

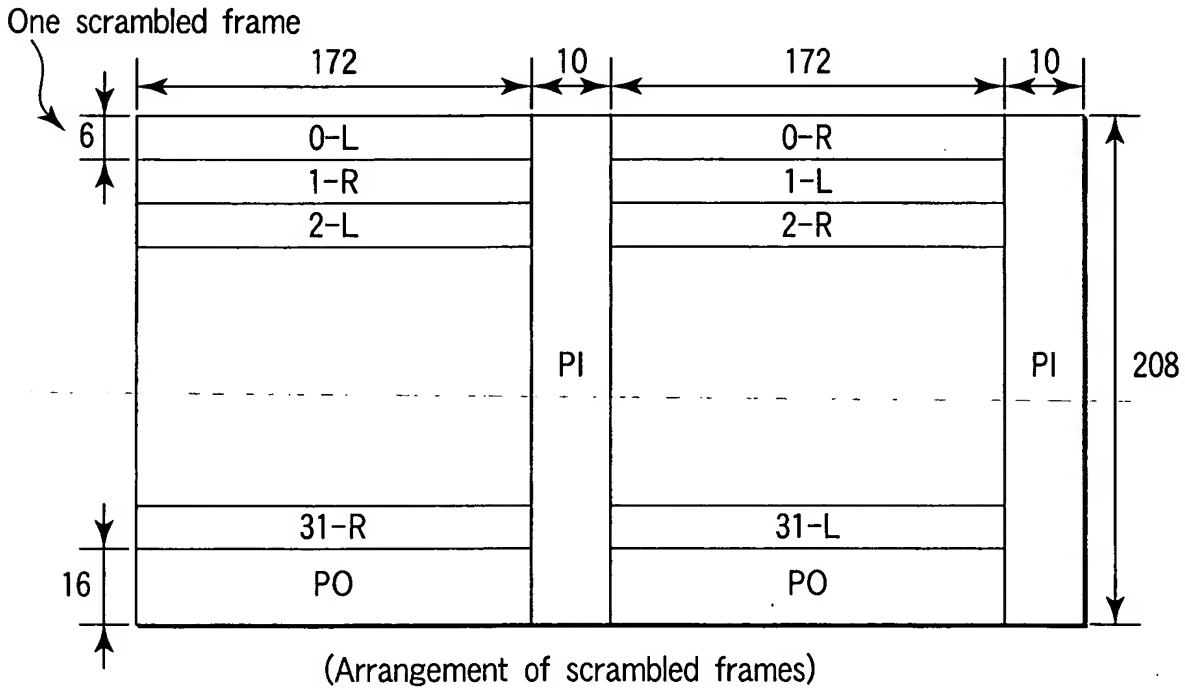


Feedback register

	172 bytes			PI 10 bytes		172 bytes			PI 10 bytes
192 rows	B0,0	B0,171	B0,172	B0,181	B0,182	B0,353	B0,354		B0,363
	B1,0	B1,171	B1,172	B1,181	B1,182	B1,353	B1,354		B1,363
	B2,0	B2,171	B2,172	B2,181	B2,182	B2,353	B2,354		B2,363
	B189,0	B189,171	B189,172	B189,181	B189,182	B189,353	B189,354		B189,363
	B190,0	B190,171	B190,172	B190,181	B190,182	B190,353	B190,354		B190,363
	B191,0	B191,171	B191,172	B191,181	B191,182	B191,353	B191,354		B191,363
PO 16 rows	B192,0	B192,171	B192,172	B192,181	B192,182	B192,353	B192,354		B192,363
	B207,0	B207,171	B207,172	B207,181	B207,182	B207,353	B207,354		B207,363

(ECC block structure)

FIG. 21



(Arrangement of scrambled frames)

FIG. 22

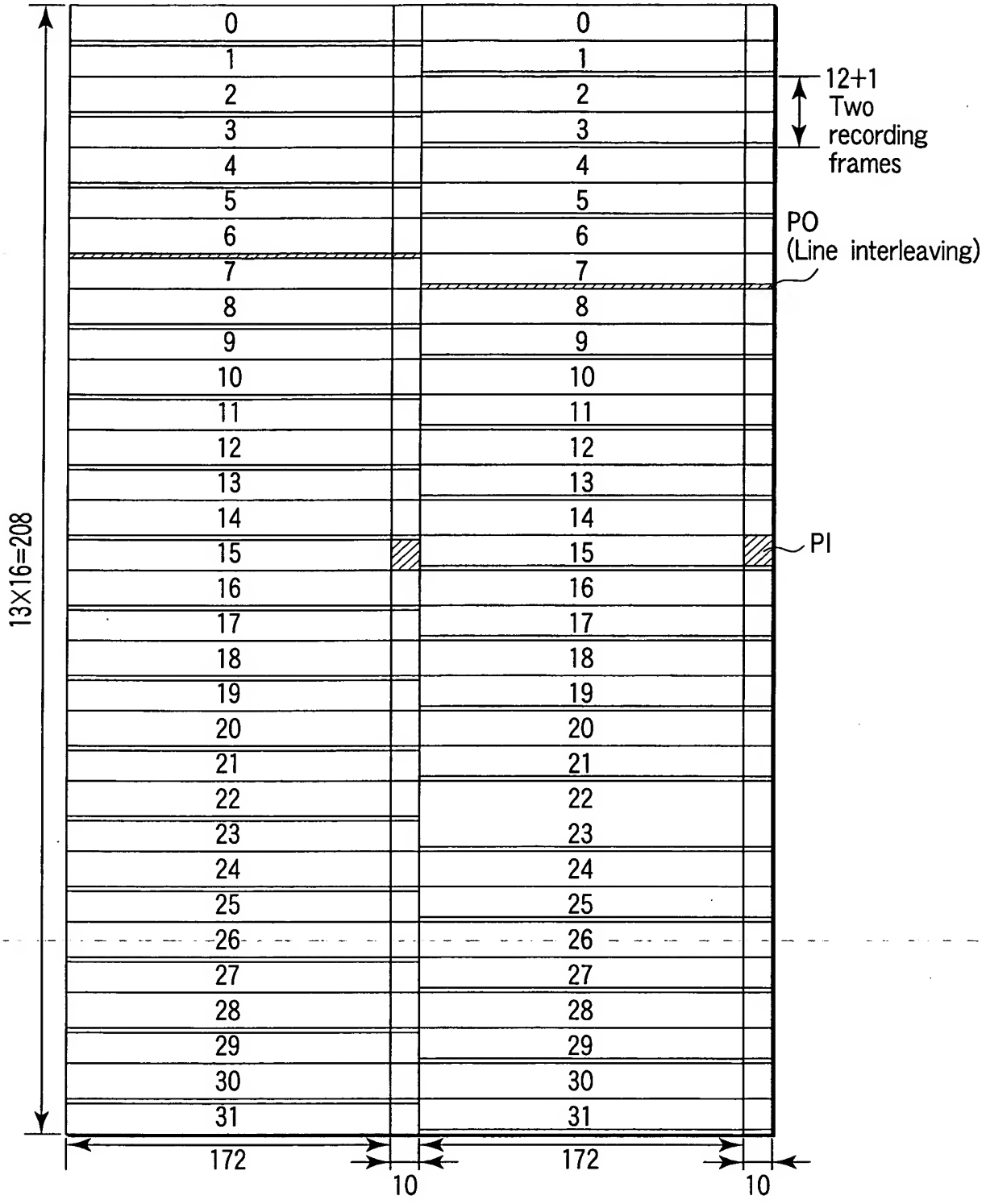

0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
12+1
Two
recording
frames
PO
(Line interleaving)
PI
13X16=208
172
10
172
10

FIG. 23

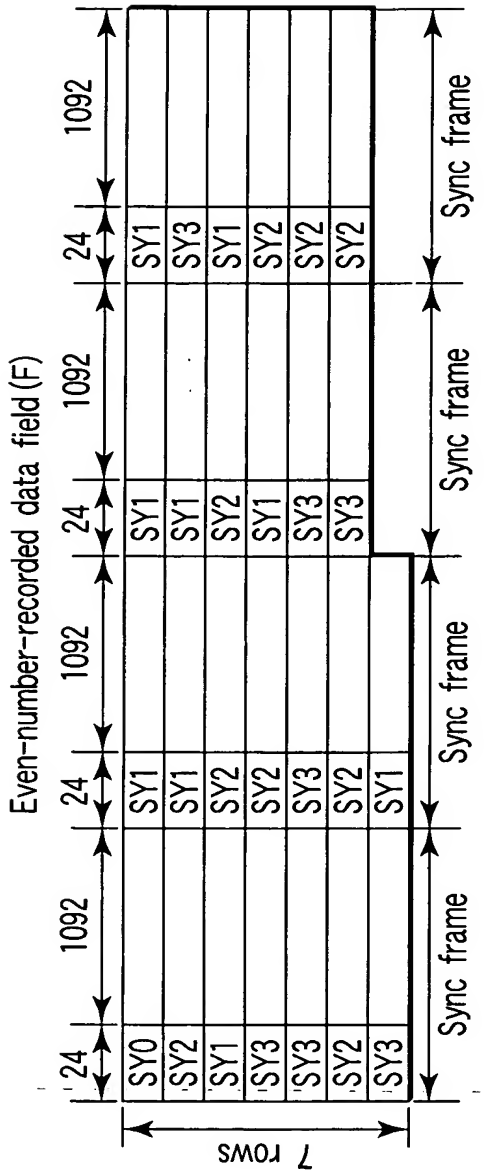


FIG. 24A

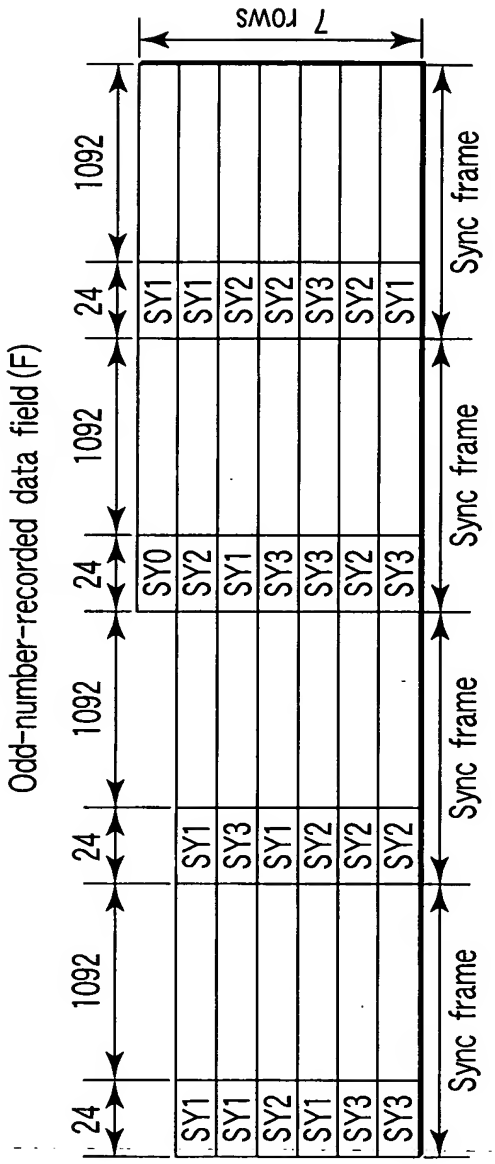


FIG. 24B

FIG. 25

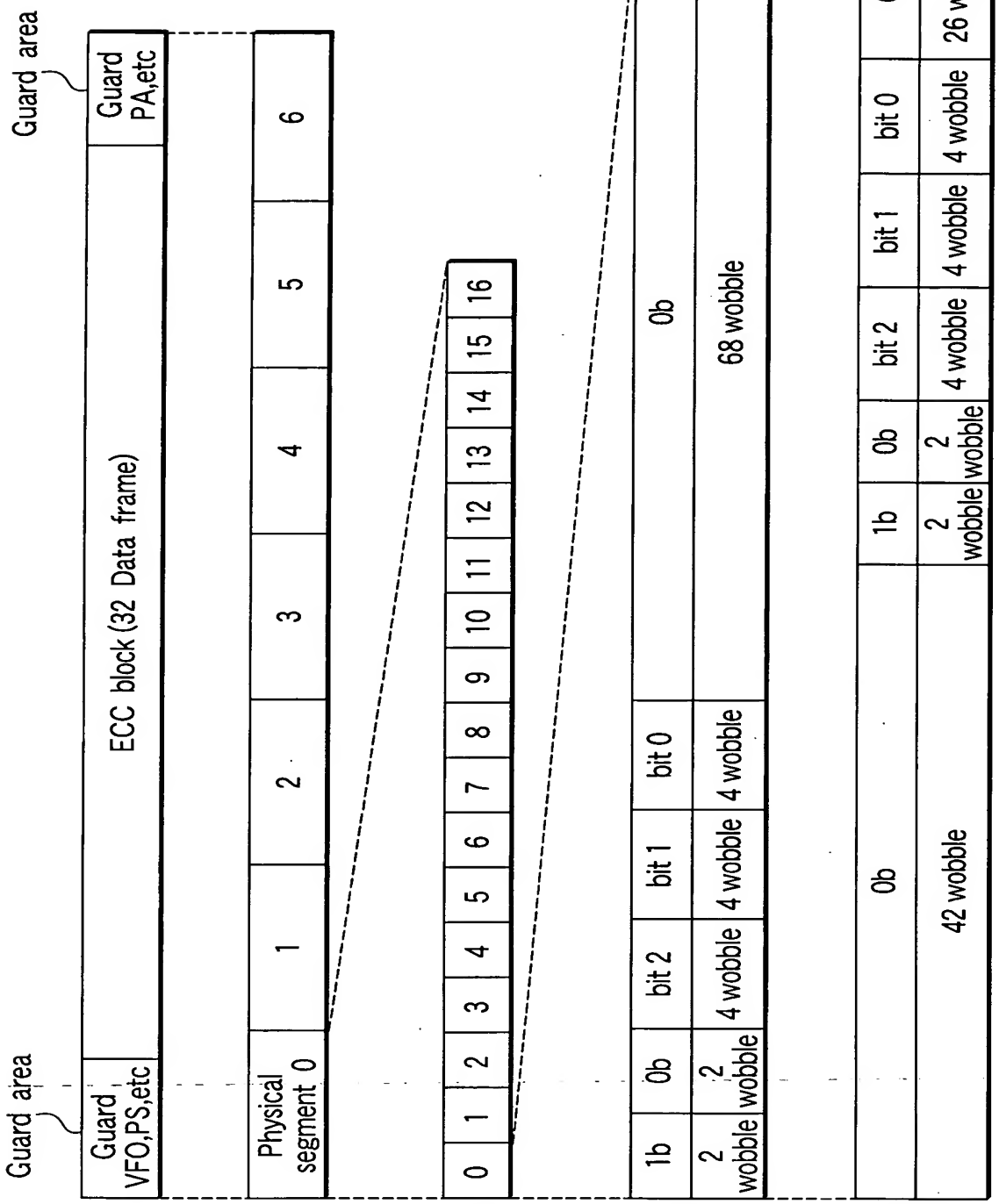
State0

		(MSB) Primary SYNC codes (LSB)					(MSB) Secondary SYNC codes (LSB)			
SY0	=	000010	101000	000000	001001	/	000010	001000	000000	001001
SY1	=	100001	001000	000000	001001	/	100010	101000	000000	001001
SY2	=	100100	001000	000000	001001	/	101000	101000	000000	001001
SY3	=	101000	001000	000000	001001	/	101010	001000	000000	001001

State1

		(MSB) Primary SYNC codes (LSB)					(MSB) Secondary SYNC codes (LSB)			
SY0	=	000100	101000	000000	001001	/	000100	001000	000000	001001
SY1	=	001001	001000	000000	001001	/	001010	101000	000000	001001
SY2	=	010000	101000	000000	001001	/	010000	001000	000000	001001
SY3	=	010100	001000	000000	001001	/	010101	001000	000000	001001

(SYNC code)


Guard area
Guard VFO,PS,etc
ECC block (32 Data frame)
Guard PA,etc
Guard area
Data segment format
FIG. 26A
Physical segment 0
1
2
3
4
5
6
FIG. 26B
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
Physical segment format
FIG. 26C
1b
0b
bit 2
bit 1
bit 0
4 wobble
0b
68 wobble
2 wobble
2 wobble
Wobble data unit (Primary)
FIG. 26D
0b
1b
0b
bit 2
bit 1
bit 0
0b
42 wobble
2 wobble
2 wobble
4 wobble
4 wobble
4 wobble
26 wobble
Wobble data unit (Secondary for R)
FIG. 26E

(Primary) (Layout of wobble data unit)

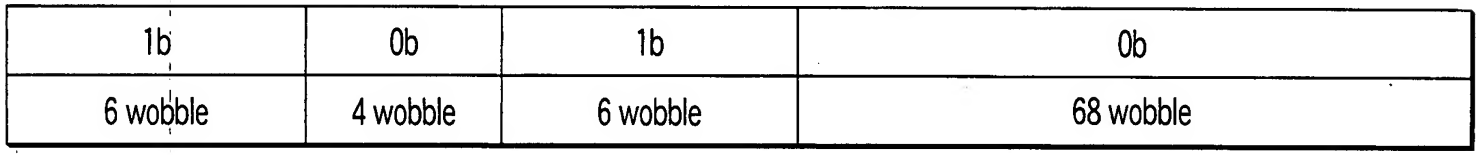


FIG. 27A

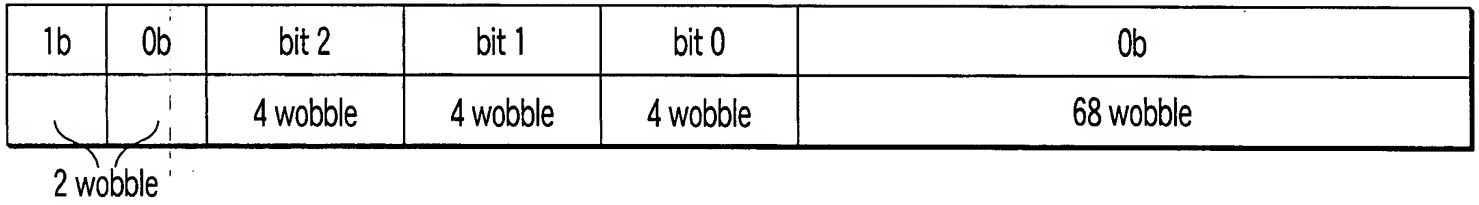


FIG. 27B

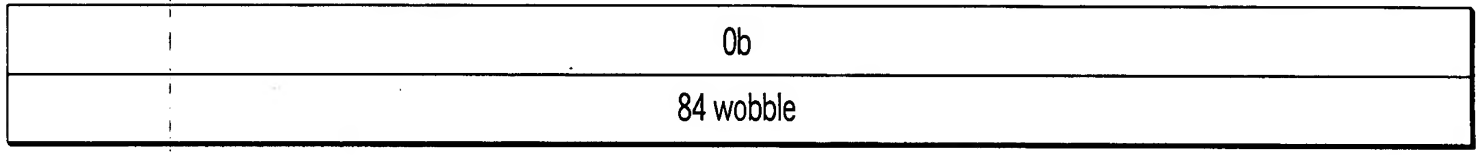


FIG. 27C

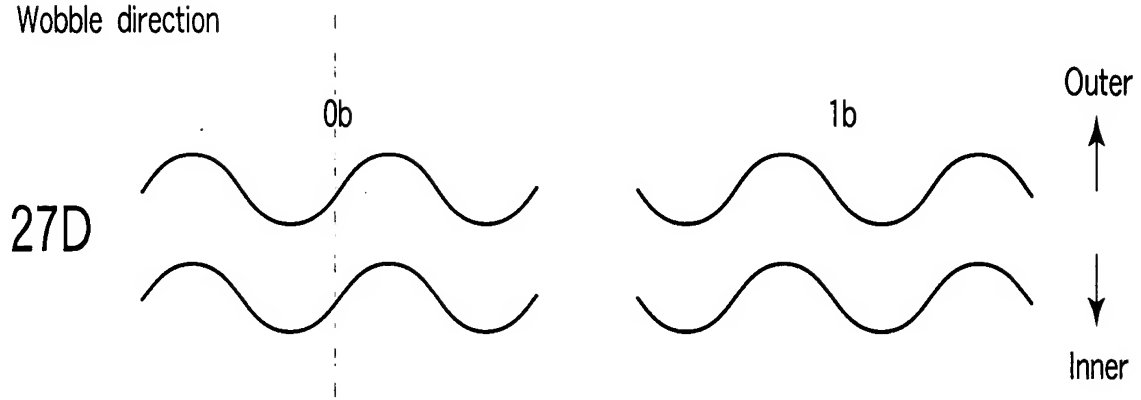


FIG. 27D

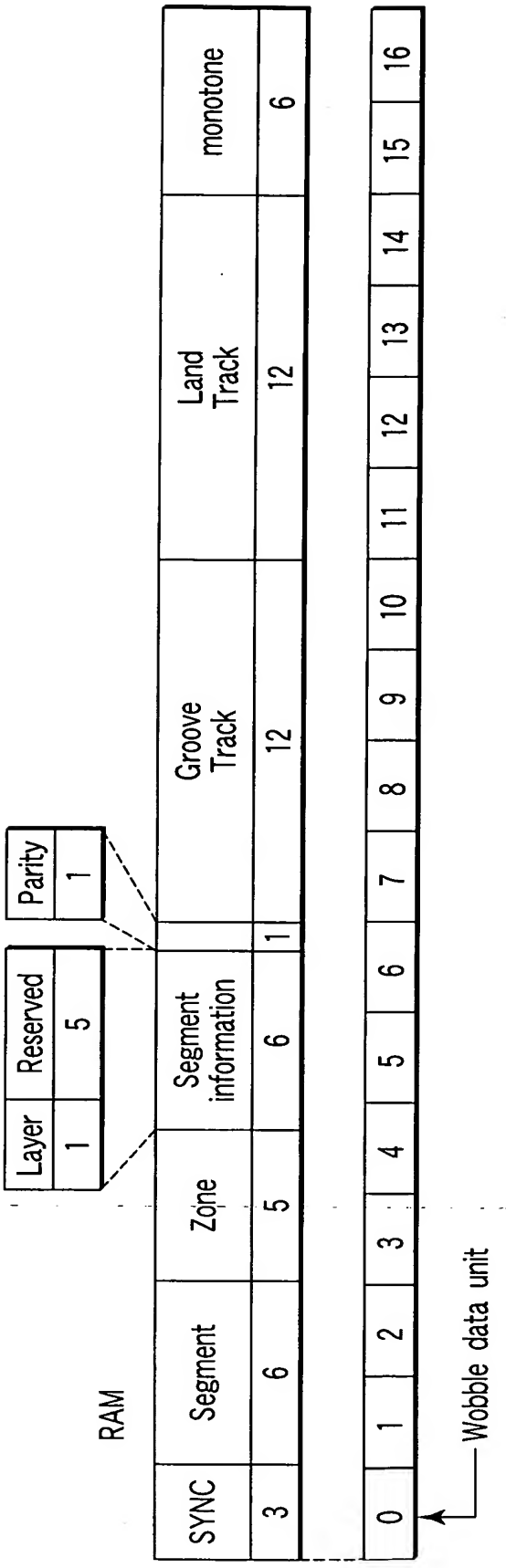


FIG. 28A

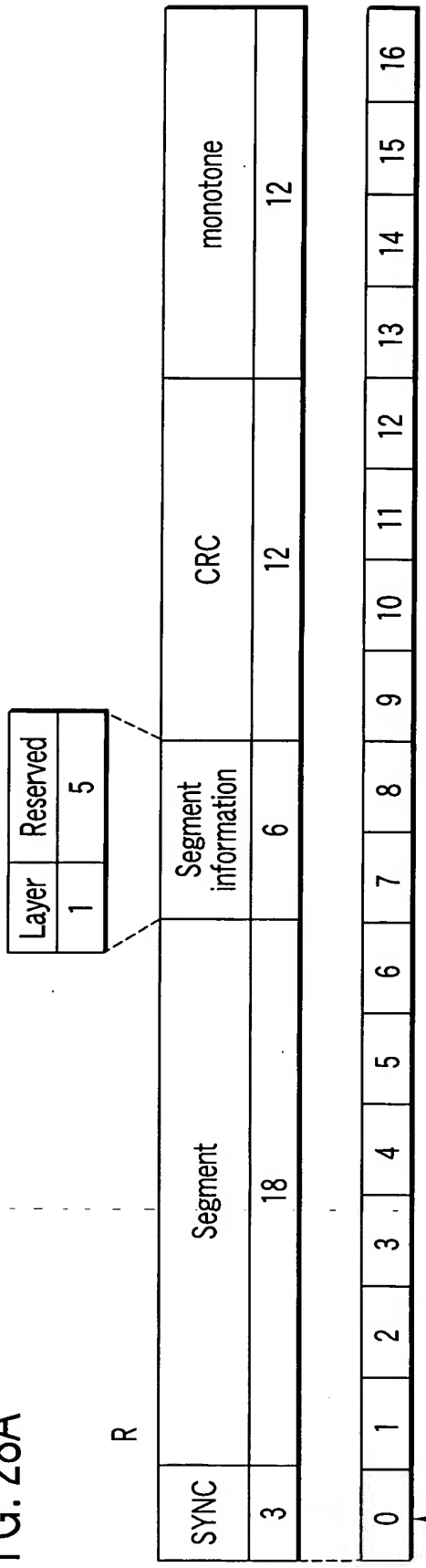


FIG. 28B

Outer edge of disk

↑

Groove	SYNC	Segment	Zone	Segment information	Parity	Groove track (m+2)	-	monotone
Land	SYNC	Segment	Zone	Segment information	Parity	-	Land track (m+2)	monotone
Groove	SYNC	Segment	Zone	Segment information	Parity	Groove track (m+1)	-	monotone
Land	SYNC	Segment	Zone	Segment information	Parity	-	Land track (m+1)	monotone
Groove	SYNC	Segment	Zone	Segment information	Parity	Groove track (m)	-	monotone
Land	SYNC	Segment	Zone	Segment information	Parity	-	Land track (m)	monotone

↓

Inner edge of disk

FIG. 29

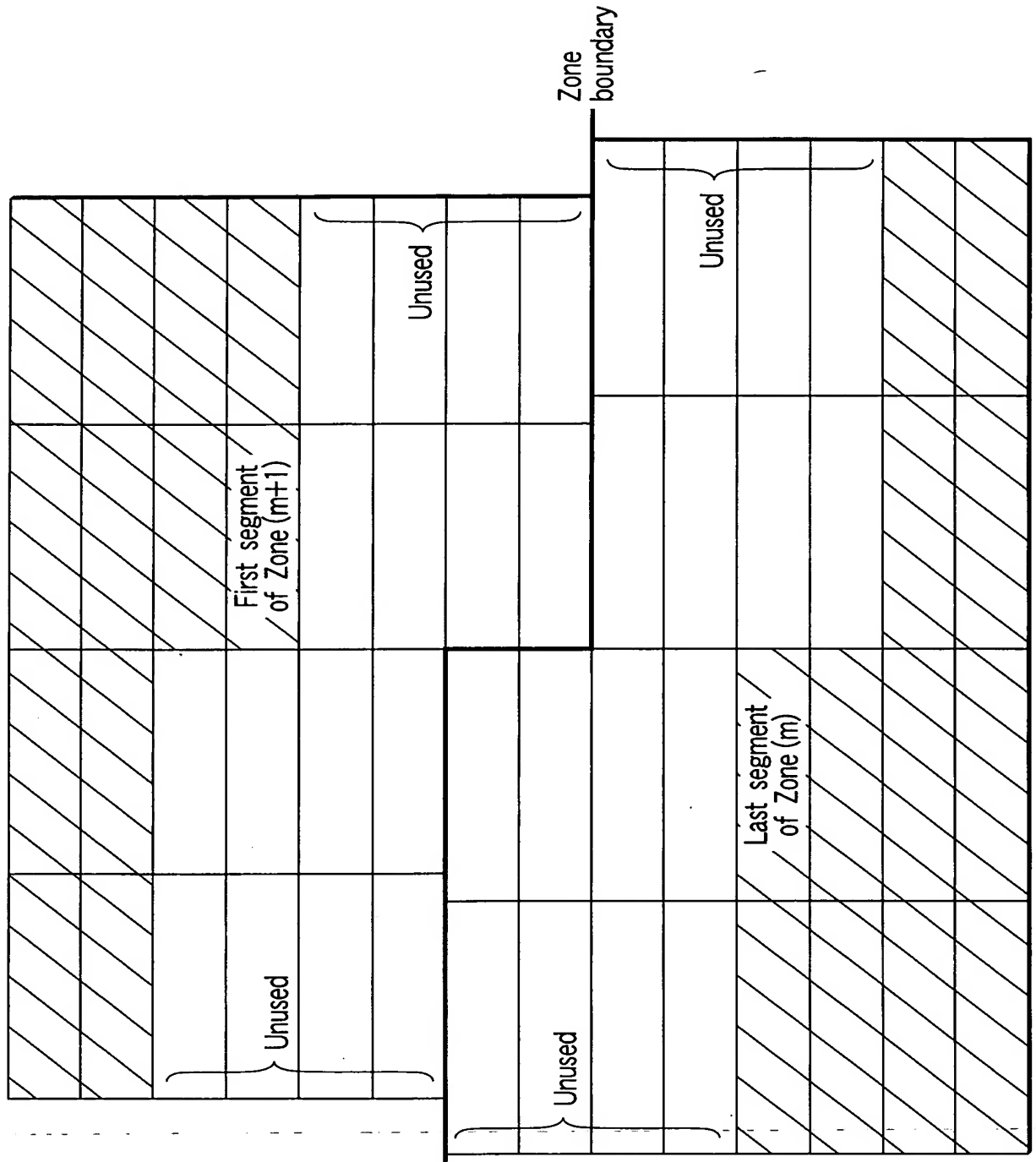

Outer edge of disk
Groove
Land
Groove
Land
Groove
Land
Groove
Land
Groove
Land
Groove
Land
Groove
Land
Inner edge of disk
Unused
First segment of Zone (m+1)
Unused
Zone boundary
Unused
Last segment of Zone (m)
Unused

FIG. 30

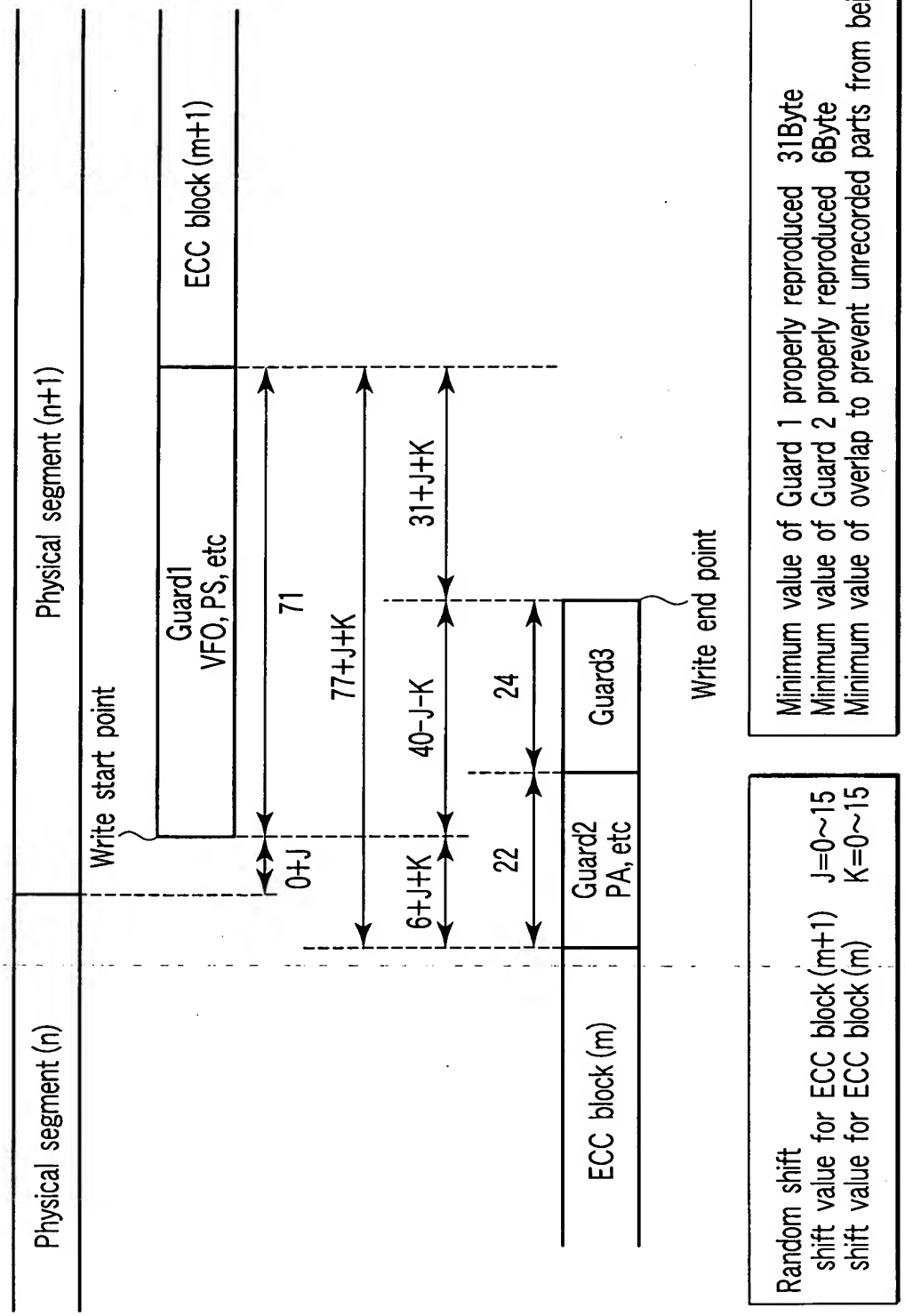

Physical segment (n)
Physical segment (n+1)
Write start point
Guard1
VFO, PS, etc
ECC block (m+1)
0+J
71
77+J+K
6+J+K
40-J-K
22
24
31+J+K
Guard2
PA, etc
Guard3
ECC block (m)
Write end point
Random shift
shift value for ECC block (m+1) J=0~15
shift value for ECC block (m) K=0~15
Minimum value of Guard 1 properly reproduced 31Byte
Minimum value of Guard 2 properly reproduced 6Byte
Minimum value of overlap to prevent unrecorded parts from being left 8Byte

FIG. 31

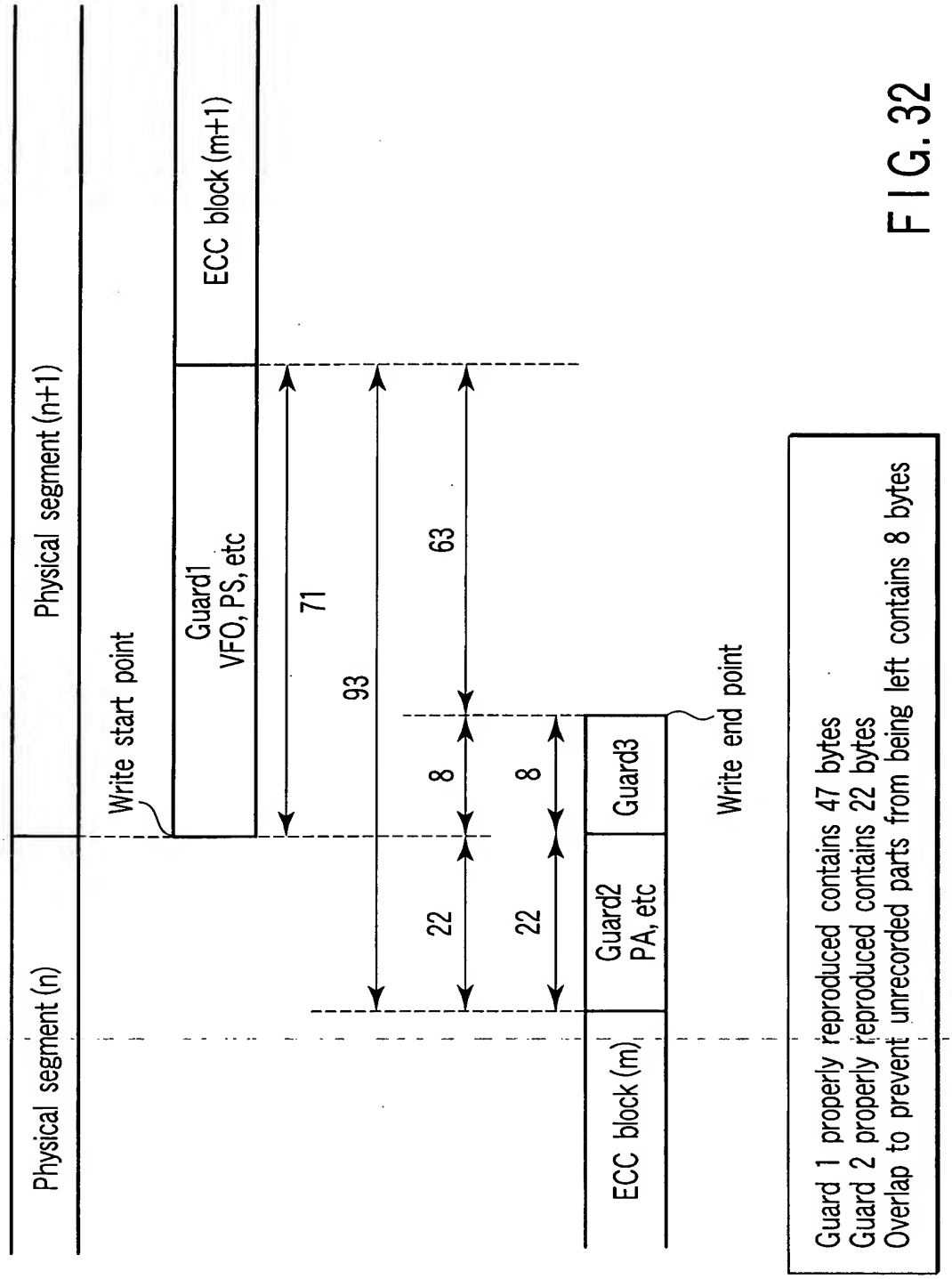

Physical segment (n)
Physical segment (n+1)
Write start point
ECC block (m+1)
Guard1
VFO, PS, etc
71
93
63
8
8
22
22
Guard2
PA, etc
Guard3
Write end point
ECC block (m)
Guard 1 properly reproduced contains 47 bytes
Guard 2 properly reproduced contains 22 bytes
Overlap to prevent unrecorded parts from being left contains 8 bytes

FIG. 32

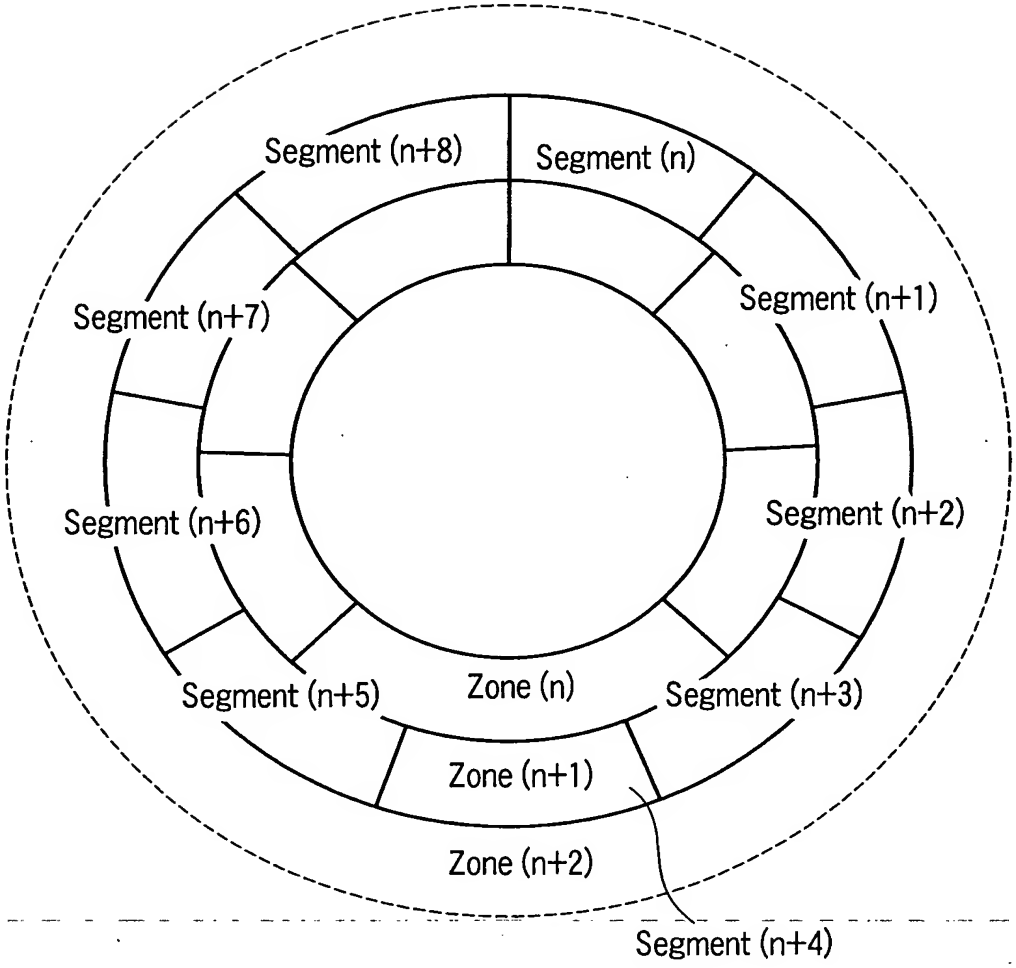
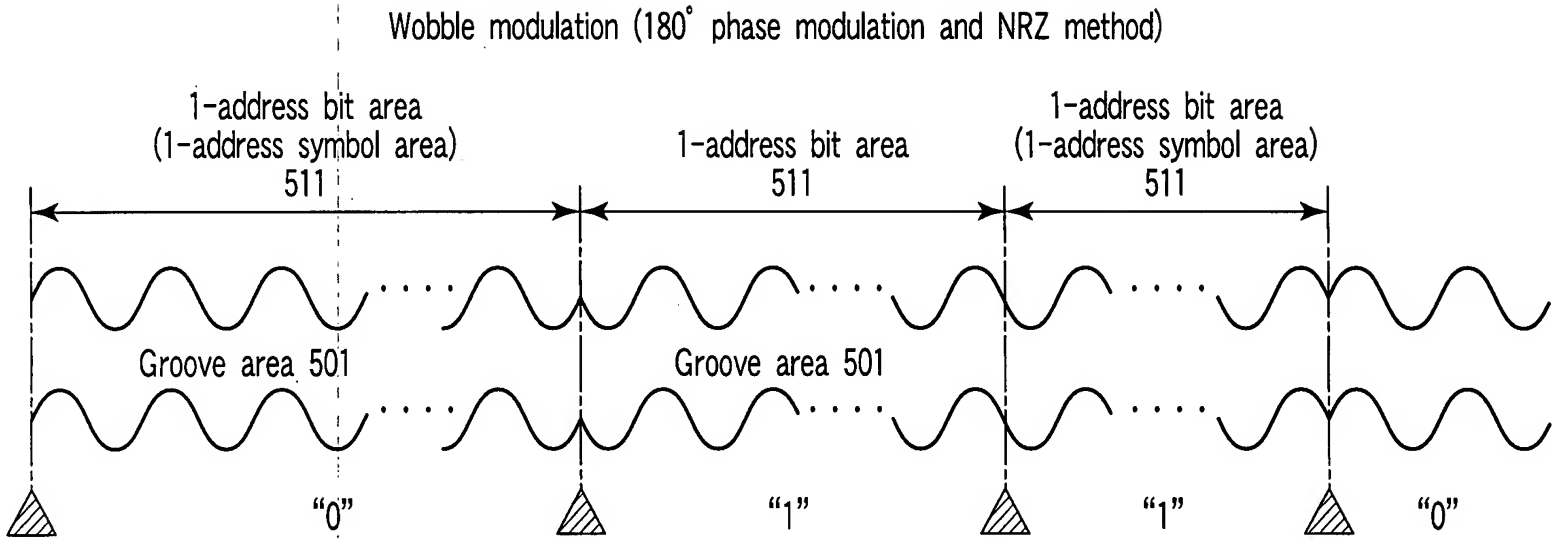

Segment (n+8)
Segment (n)
Segment (n+1)
Segment (n+7)
Segment (n+6)
Segment (n+2)
Segment (n+5)
Zone (n)
Segment (n+3)
Zone (n+1)
Zone (n+2)
Segment (n+4)

FIG. 33



☆ 1-address bit area 511 (expressed in 8 wobbles or 12 wobbles)
☆ Frequency, amplitude, and phase in 1-address bit area = constant everywhere
☆ Boundary part of 1-address bit area 511 (180° or 0° phase shift)

FIG. 34

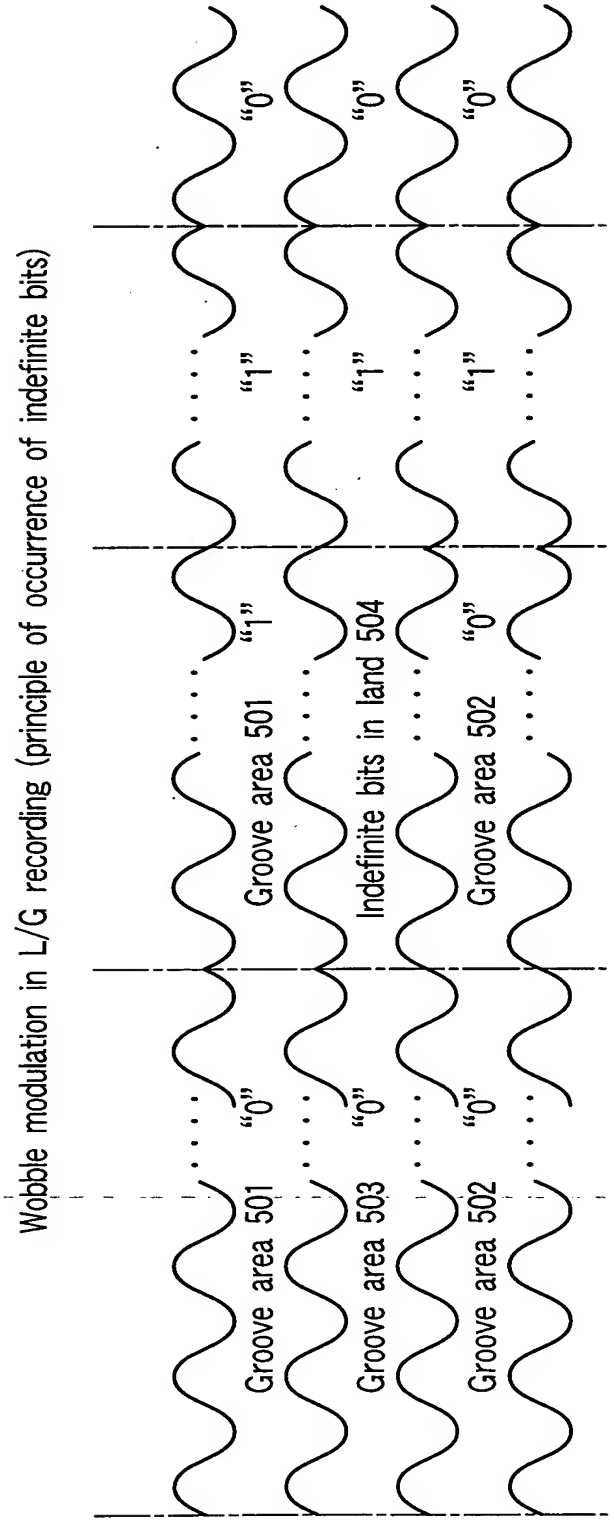

Wobble modulation in L/G recording (principle of occurrence of indefinite bits)
Groove area 501
Groove area 503
Groove area 502
"0"
"1"
Groove area 501
Indefinite bits in land 504
Groove area 502

FIG. 35

Example of Gray code

Decimal number	Conventional binary representation	Gray code representation
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

FIG. 36

(Configuration of information recording and reproducing apparatus) (particularly centering on the recording system)

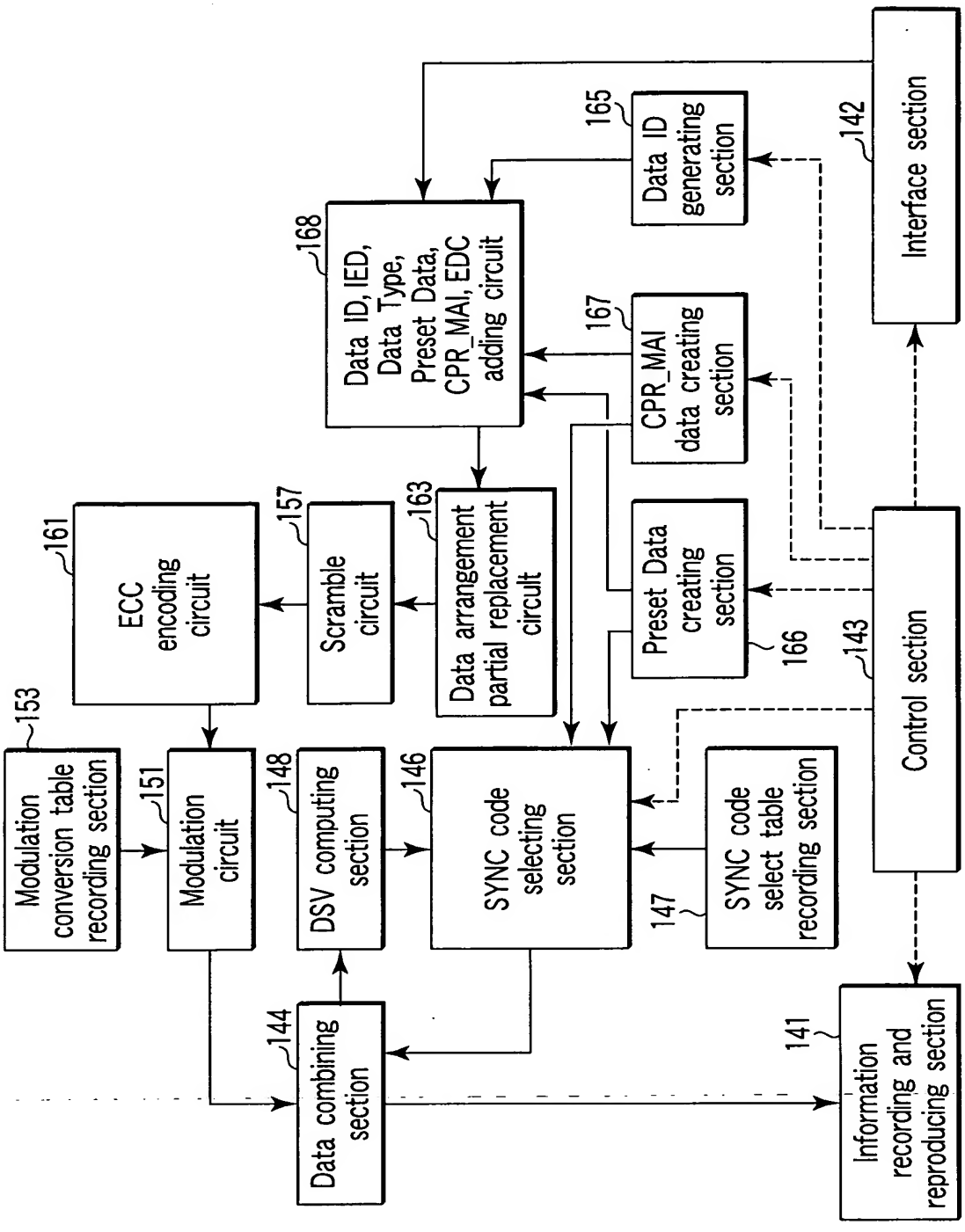


FIG. 37

(Configuration of information recording and reproducing apparatus) (particularly centering on the reproducing system)

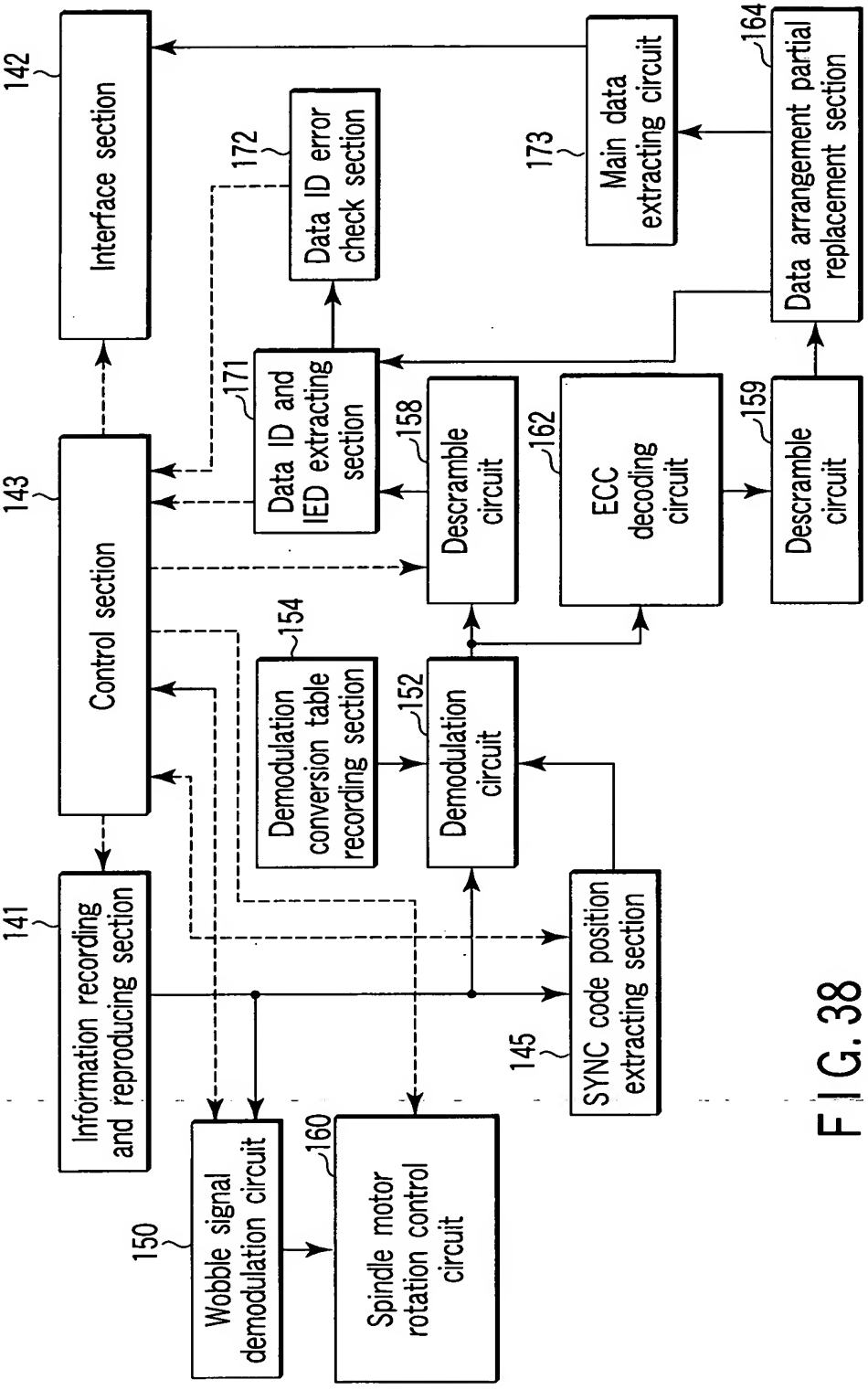


FIG. 38